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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/668,999	09/25/00	BRODSKY J	TI-31026

EXAMINER	
FARAHANI, D	
ART UNIT	**PAPER NUMBER**
2814	

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DATE MAILED: 11/02/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/668,999	BRODSKY ET AL.	
	Examiner	Art Unit	
	Dana Farahani	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2000* .

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-24* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims1-17 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Pan (U.S. 6281554B1).

Regarding claims 1 and 10, Pan discloses, in figure 4, an input/output (I/O) pad in the left center of the figure, an interface circuit, at the right end of the figure, connected to the I/O pad. A charge device model clamp circuit, 144 and 146, is connected to the I/O pad and the interface circuit. The charge device model clamp circuit and the interface circuit are adjacent to each other and share a common device element by a V_{DD} line at the top of the figure.

Regarding claim 2, Pan discloses, in figure 4, a resistor, in the center of the figure, disposed between the input/output pad and the interface circuit.

Regarding claim 3, the charge device model clamp circuit of figure 4 comprises a first transistor, 144, and the interface circuit comprises a second transistor at the top right of the figure below the V_{DD} line.

Regarding claims 4 and 11, the first and the second mentioned transistors are MOS transistors.

Regarding claims 5 and 12, the charge device model clamp circuit and the interface circuit share a common source region connected by the V_{DD} line (see figure 4).

Regarding claims 6 and 13, the I/O pad is an input pad and the interface circuit is an input circuit.

Regarding claims 7 and 14, the charge device model clamp circuit comprises a first PMOS transistor, 144 of figure 4, and the interface circuit comprises a second PMOS transistor, at the top right of the figure, below the V_{DD} line, and the common device element is a P+ source region 112 of figure 3.

Regarding claims 8 and 15, the charge device model clamp circuit, 144 and 146 of figure 4, comprises a first NMOS transistor 146, and the interface circuit comprises a second NMOS transistor, shown at the right bottom of the figure, above a Vss line, and the common device element is an n+ source region, 134 of figure 3, connected by the Vss line.

Regarding claims 9 and 16, the charge device model clamp circuit of figure 4, comprises a first PMOS transistor, 144, and a first NMOS transistor, 146, the interface circuit comprises a second PMOS transistor, shown at the top right of the figure, below the V_{DD} line, and a second NMOS transistor, shown at the bottom right of the figure, above the Vss line, wherein the first and the second PMOS transistors share a P+ source region, connected by the V_{DD} line, and the first and the second NMOS transistors share an N+ source region, connected by the V_{SS} line.

Regarding claims 17 and 21, Pan discloses, in figure 3, a semiconductor substrate 100; a first drain region, 138, disposed in the substrate 100; a first channel

region (not shown) to the right of the drain region 138; a first gate dielectric overlying the first channel region; a gate, 136, overlying the first gate dielectric; a first source region, 134, disposed in the substrate 100 directly adjacent to the first channel region; a second channel region (not shown) in substrate 100 directly adjacent to the source region 134 on a side of the source region 134 opposite to the first channel region; a second gate dielectric overlying the second channel region; second gate,128, overlying the second gate dielectric; a second drain region, 126, disposed in the substrate 100 directly adjacent to the second channel region.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims18, 22, 19-20 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan, as applied to claims 17 and 21 above, and further in view of Utsunomiya et al.

Regarding claims 18 and 22, Pan discloses, in figure 3, the input/output pad 118 connected to the drain region 126. However, Pan does not disclose the input/output pad connected to the gate 136. Utsunomiya discloses a structure for static electricity protection in which an input/output pad, 103 of figure 1, is connected to the gate region of transistor 105, and the drain region of the transistor 104, so the gate is prevented

from being damaged. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to connect the input/output pad Pan discloses to the first gate region in order to prevent the gate from being damaged.

Regarding claims 19-20 and 23-24, Pan discloses an N-type substrate 100 and N+ source and drain regions 126, 134 and 138. However, Pan does not disclose a P-type substrate or a P-well around the source and drain regions. It is well known in the art to use N-type or P-type substrates, interchangeably, and N-type or P-type wells, interchangeably, and P+ or N+ source and drain regions in order to make PMOS or NMOS transistors (see, for example, Streetman and Banerjee, page289, figure 6-27a, and 6-27b). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a P-type substrate and an N-well in Pan's invention in order to make NMOS or PMOS transistors.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (703)305-1914. The examiner can normally be reached on M-F 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703)306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703)305-3432 for regular communications and (703)305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Dana Farahani
October 30, 2001

OLIK CHAUDHURI
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